WHAT IS CLAIMED IS:

1. Apparatus for synchronizing a regularly occurring pulse train in frequency to the average of a bunched pulse train, the apparatus comprising:

means for generating from an oscillator a plurality of differently phase shifted signals at a given frequency;

a multiplexer that generates an output signal from a selected one of its input signals;

means for applying the phase shifted signals to the input of the multiplexer such that the multiplexer phase shifted signals;

a FIFO;

means for filling the FIFO with the bunched pulse train;

means for emptying the FIFO at the frequency of the output signal from the multiplexer;

means for generating an error signal that represents the state of the FIFO;

means for filtering the error signal;

means for accumulating the filtered error signal to produce a phase selection signal; and

means for applying the one phase shifted signal to the multiplexer responsive to the phase selection signal so the output signal occurs at the average frequency of the bunched pulse train.

2. The apparatus of claim 1, in which the means for generating a plurality of differently phase shifted signals comprises a plurality of differential amplifier stages and means for coupling the differential amplifier stages together

to form a ring oscillator, the phase shifted signals being generated by the respective stages such that each stage produces two signals shifted in phase 180° from each other.

3. The apparatus of claim 2, in which the differential amplifier stages have equal controllable delays.

4. The apparatus of claim 3, in which the coupling means couples eight differential amplifier stages together such that sixteen differently phase shifted signals are generated.

5. The apparatus of claim 4, in which the accumulating means accumulates the filtered error signal at the frequency of the output signal.

6. The apparatus of claim 1, in which the phase shifted signals have two binary values and the changing means changes from one phase shifted signal to another phase shifted signal when both phase shifted signals have the same binary value.

7. The apparatus of claim 1, in which the means for generating a plurality of differently phase shifted signals comprises means for synchronizing the oscillator to a stable frequency reference.

8. The apparatus of claim 7, in which the synchronizing means comprises a phase locked loop that has a number of counters with programmable dividing factors that determine the frequency of the phase shifted signals and means for programming the counters to establish the desired frequency.

9. The apparatus of claim 8, in which the phase locked loop has a broad bandwidth.

10. The apparatus of claim 9, in which the filtering means comprises a control loop that has a narrow bandwidth.

11. The apparatus of claim 1, additionally comprising means for adding a frequency offset to the filtered error signal prior to accumulating the filtered error signal.

12. The apparatus of claim 11, in which the frequency offset is selected to minimize the correction made by the multiplexer.

13. Apparatus for synchronizing a regularly occurring clock pulse train in frequency to the average of a bunched clock pulse train corresponding to data, the apparatus comprising:

a FIFO having a given number of storage locations, an empty flag storage cell for each location, and a full flag storage cell for each location;

an oscillator producing as an output signal the regularly occurring clock pulse train;

means for filling the FIFO with the data responsive to the bunched clock pulse train and emptying the FIFO responsive to the output signal;

means for producing an error signal that represents the state of the FIFO;

means for setting an empty flag in the empty flag storage cell of a storage location and resetting a full flag in the

full flag storage cell of the storage location when data is read out of the corresponding storage location;

means for setting a full flag in the full flag storage cell of a storage location and resetting an empty flag in the empty flag storage cell of the storage location when data is written into the corresponding storage location;

means for summing either the empty flags or the full flags to produce an error signal that represents the state of the FIFO; and

means for applying the error signal to the oscillator to change the frequency of the output signal so the state of the FIFO remains approximately constant.

14. The apparatus of claim 13, additionally comprising means for adding a frequency offset to the error before the error signal is applied to the oscillator.

15. The apparatus of claim 14, in which the frequency offset is selected to minimize the correction made to the oscillator.